REMARKS

This amendment is submitted in response to an Office Action mailed October 23, 2002. Applicant respectfully requests reconsideration of the subject application as amended herein.

Claims 1-9 remain in the present application. Claims 10-20 have been added to the present application.

As part of this amendment, Applicant has amended claims 1-9 to correct previously undetected informalities. The amendments to claims 1-9 have not been made to overcome a statutory rejection, and therefore no element has lost any equivalence under the Doctrine of Equivalence.

The summary page of the October 23, 2002 Office Action indicated that the specification was objected to. However, the detailed action made no mention of an objection to the specification. Applicant assumes that no objection to the specification was intended.

The specification has been amended to correct a previously undetected informality. No new matter has been added.

In the October 23, 2002 Office Action, claims 1-9 were rejected under 35 U.S.C. § 103 as being unpatentable over U.S. Patent No. 6,064,247 issued to Krakirian (hereinafter "Krakirian") in view of U.S. Patent No. 5,701,441 issued to Trimberger (hereinafter "Trimberger"). As discussed below, Applicant

respectfully submits that claims 1-9 are patentable over Krakirian in view of Trimberger.

For example, claim 1 includes:

> A method for clock generation and distribution in an emulation system comprising:
> generating a derived clock signal from a look up table, wherein an index to the look up table is generated by counting cycles of a base clock signal;
> stopping emulation by stopping the base clock signal, wherein the index to the look up table is stopped at a stopping point in a clock cycle of the derived clock signal and the derived clock signal does not continue to a subsequent transition before stopping; and
> resuming emulation by resuming the base clock signal, wherein the derived clock signal is resumed at the stopping point in the clock cycle of the derived clock signal.

In claim 1, a clock signal is derived from a base clock signal by counting cycles in the base clock signal and then using the number of counted cycles as an index to a look up table. The output from the look up table is the derived clock.

Krakirian, in contrast, derives a clock signal (C) from an input clock (CIN) using an AND gate, an OR gate, and two control signals (CnH and CnL) (Krakirian: Figure 3; col. 4, lines 12-15). The control signals are generated using an elaborate circuit of registers (element 690) that are interconnected in any of a variety of ways, none of which have anything to do with counting cycles in the input clock signal (Krakirian: Figures 6A - 6F; cols. 6-8).

The Office Action asserts at the end of page 1 to the top of page 2:

> Krakirian discloses ... generating a derived clock signal from a look up table, wherein an index to the look up table is generated by

counting cycles of a base clock signal (See Col. 4, lines 39 et Seq, Table 1.... Also see Col. 2, lines 25 et Seq....)

Table 1, however, is merely a truth table that describes the logical function of the three-input, one-output AND/OR circuit mentioned above. The three inputs are the input clock (CIN), and the two control signals (CnH and CnL). The output is the derived clock (Cn). Table 1 defines all possible combinations of the three inputs and the resulting output.

The text at Col. 4, lines 39 et Seq merely elaborates on how the control lines can force the output high or low in the AND/OR circuit described by Table 1. The text at Col. 2, lines 25 et Seq merely describes how an input clock can be frequency divided.

Assuming purely for the sake of argument that the AND/OR circuit described by Table 1 could be considered a look up table, then the three inputs would be the index to the table. The most significant bit of the three inputs, however, is the input clock (CIN) itself. Clearly the three inputs are not generated by counting the number of cycles in the input clock. Put another way, Krakirian does not suggest, disclose, or enable that "an index to the look up table is generated by counting cycles of a base clock signal," as claimed in claim 1.

Trimberger was cited for teaching stopping and restarting emulation. Trimberger has nothing whatsoever to do with generating a derived clocked. Therefore, Applicant respectfully submits that Trimberger does not cure the deficiencies of Krakirian.

Thus, for at least the reasons discussed above, Applicant respectfully submits that claim 1 is not obvious in light of Krakirian in view of Trimberger.

Applicant submits that the reasoning presented above with respect to claim 1 similarly applies to claims 3 and 8. Thus, for at least the reasons discussed above, Applicant respectfully submits that claims 3 and 8 are likewise not obvious in light of Krakirian in view of Trimberger.

Given that claim 2 depends from claim 1, claims 4-7 depend from claim 3, and claim 9 depends from claim 8, Applicant respectfully submits that claims 2, 4-7, and 9 are likewise not obvious in light of Krakirian in view of Trimberger for at least the reasons discussed above.

Applicant respectfully submits that the reasoning presented above similarly applies to new claims 10-20. Therefore, for at least the reasons discussed above, Applicant respectfully submits new claims 10-20 are patentable over the cited references.

In conclusion, Applicant respectfully submits that claims 1-20 are now in a condition for allowance, and Applicant respectfully requests allowance of such claims.

Please charge any shortages and credit any overages to our Deposit Account No. 500393.

Respectfully submitted,

SCHWABE, WILLIAMSON & WYATT, PC

Date: 1/23, 2003

Robert A. Diehl
Reg. No. 40,992

10260 SW Greenburg Road, Suite 820
Portland, Oregon 97223
Phone: (503) 595-2800
FAX: (503) 595-2804

MARKED VERSION OF AMENDMENTS TO SHOW CHANGES MADE

IN THE SPECIFICATION

Please amend the specification as follows:

The paragraph at page 7, lines 16-27

In one embodiment, frequency multiplier 220 is coupled between an external clock signal and multiplexor 210. Frequency multiplier 220 multiplies the external clock signal by the appropriate factor to compensate for frequency divider circuit 152 and look up table 156 such that one or more of the derived clock signals has a frequency equal to the external clock signal. By multiplying the external clock signals, the circuitry in derived clock generation circuit 150 may be shared by the external clock signal and the base clock signal. However, transients in the external clock signal are passed ~~though~~ through derived clock generation circuit 150 to the output signal. This provides the proper relationship between the external clock signal and the derived clock signals regardless of inconsistencies and/or transients in the external clock signal or the base clock signal, and the ability to start, stop and resume the derived clock signal at points in addition to clock edges.

IN THE CLAIMS

Please amend the claims as follows:

1. (Once Amended) A method for clock generation and distribution in an emulation system comprising:

generating a derived clock signal from a look up table, wherein an index to the look up table is generated by counting cycles of a base clock signal;

stopping emulation by stopping the base clock signal, wherein the index to the look up table is stopped at a stopping point in a clock cycle of the derived clock ~~cycle~~ signal and the derived clock signal does not continue to a subsequent transition before stopping; and

resuming emulation by resuming the base clock signal, wherein the derived clock signal is resumed at the stopping point in the clock cycle of the derived clock signal ~~cycle~~.

2. (Once Amended) The method of claim 1, wherein ~~the step of~~ generating ~~a~~ the derived clock signal further comprises:

accessing an entry in a look up table having an address corresponding to ~~the~~ a number of ~~intermediate~~ clock ~~signals~~ cycles that have been counted; and

outputting a signal level in response to the entry accessed.

3. (Once Amended) An emulation system comprising:

a plurality of emulation boards each having hardware to emulate one or more circuit designs;

means for interconnecting the plurality of emulation boards;

a clock generation circuit comprising

a base clock generation circuit that generates a base clock signal of a first frequency, and

a derived clock generation circuit having

a frequency divider circuit coupled to receive the base clock signal,

a counter circuit coupled to receive an output of the frequency divider circuit, and

a look up table coupled to receive an output of the counter circuit, wherein the output of the counter circuit is used to index entries in the look up table, and further wherein the entries in the look up table indicate a signal level for a derived clock signal generated by the clock generation circuit ~~circuitry~~.

4. (Once Amended) The emulation system of claim 3, further comprising a plurality of additional clock generation circuits coupled in parallel to generate a plurality of additional derived clock signals.

5. (Once Amended) The emulation system of claim 4, wherein the plurality of additional clock generation circuits each further comprise a selection circuit comprising a multiplexor coupled to receive the base clock signal and to receive an external clock signal from an external source, the multiplexor having an output coupled to ~~the~~ a respective frequency divider circuit, wherein a select input of the multiplexor is provided by the external source.

6. (Once Amended) The emulation system of claim 5, wherein the plurality of additional clock generation circuits each further comprise a frequency multiplier circuit that multiplies the external clock signal and provides a multiplied external clock signal to the multiplexor.

7. (Once Amended) The emulation system of claim 3, wherein the derived clock signal is distributed to the plurality of emulation boards.

8. (Once Amended) An apparatus for generating clock signals in an emulation system comprising:

means for generating a derived clock signal from a look up table, wherein an index to the look up table is generated by counting cycles of a base clock signal;

means for stopping emulation by stopping the base clock signal, wherein the index to the look up table is stopped at a stopping point in a clock cycle of

the derived clock ~~cycle~~ signal and the derived clock signal does not continue to a subsequent transition before stopping; and

means for resuming emulation by resuming the base clock signal, wherein the derived clock signal is resumed at the stopping point in the clock cycle of the derived clock signal ~~cycle~~.

9. (Once Amended) The apparatus of claim 8, wherein the means for generating a derived clock signal further comprises:

means for accessing an entry in a look up table having an address corresponding to ~~the~~ a number of ~~intermediate~~ clock ~~signals~~ cycles that have been counted; and

means for outputting a signal level in response to the entry accessed.